

MC14066B

Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — $12 \text{ nV}/\sqrt{\text{Cycle}}$, $f \geq 1.0 \text{ kHz}$ typical
- Pin-for-Pin Replacement for CD4016, MC14016B
- For Lower R_{ON} , Use The HC4066 High-Speed CMOS Device

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient) per Control Pin	± 10	mA
I_{SW}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

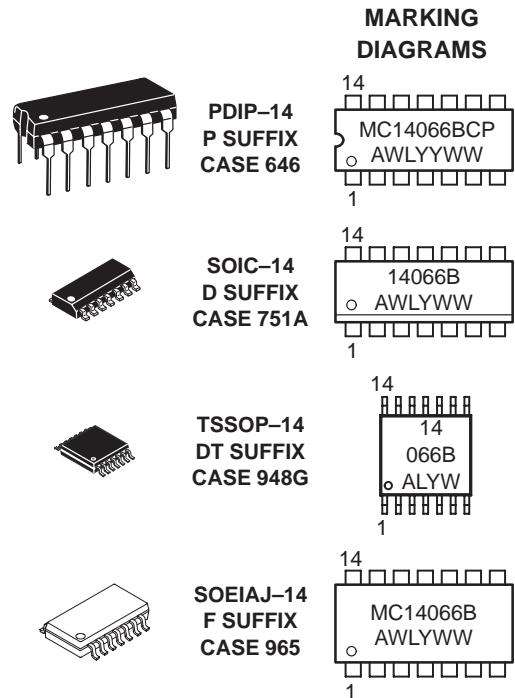
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

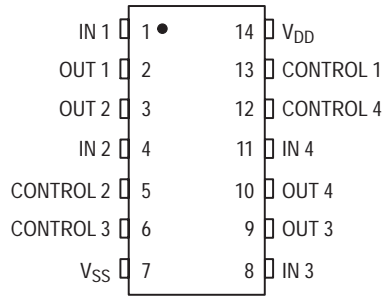
ORDERING INFORMATION

Device	Package	Shipping
MC14066BCP	PDIP-14	2000/Box
MC14066BD	SOIC-14	55/Rail
MC14066BDR2	SOIC-14	2500/Tape & Reel
MC14066BDT	TSSOP-14	96/Rail
MC14066BDTEL	TSSOP-14	2000/Tape & Reel
MC14066BDTR2	TSSOP-14	2500/Tape & Reel
MC14066BF	SOEIAJ-14	See Note 1.
MC14066BFEL	SOEIAJ-14	See Note 1.

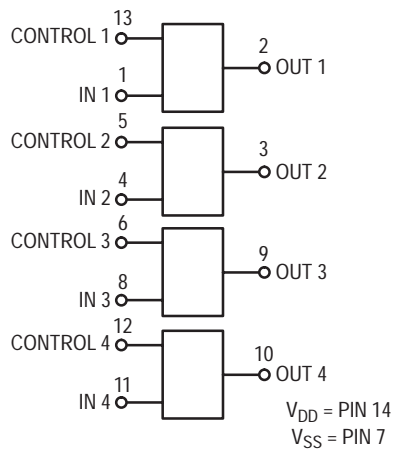
- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

MC14066B

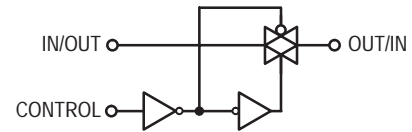
PIN ASSIGNMENT



BLOCK DIAGRAM



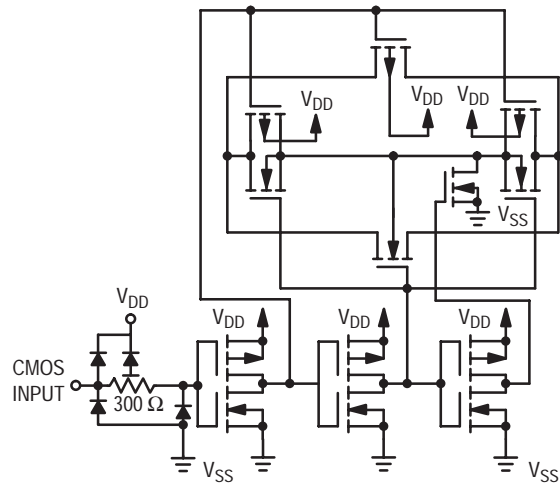
LOGIC DIAGRAM AND TRUTH TABLE (1/4 OF DEVICE SHOWN)



Control	Switch
0 = V _{SS}	OFF
1 = V _{DD}	ON

Logic Diagram Restrictions
 $V_{SS} \leq V_{in} \leq V_{DD}$
 $V_{SS} \leq V_{out} \leq V_{DD}$

CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



MC14066B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4)	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV (5.)	—	0.25	—	0.005	0.25	—	7.5	μA
		10		—	0.5	—	0.010	0.5	—	15	
		15		—	1.0	—	0.015	1.0	—	30	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only The channel component, (V _{in} - V _{out})/R _{on} , is not included.)	Typical (0.07 μA/kHz) f + I _{DD} (0.20 μA/kHz) f + I _{DD} (0.36 μA/kHz) f + I _{DD}						μA	

CONTROL INPUTS (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0	R _{on} = per spec, I _{off} = per spec	—	1.5	—	2.25	1.5	—	1.5	V
		10		—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V _{IH}	5.0	R _{on} = per spec, I _{off} = per spec	3.5	—	3.5	2.75	—	3.5	—	V
		10		7.0	—	7.0	5.50	—	7.0	—	
		15		11	—	11	8.25	—	11	—	
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN AND OUT (Voltages Referenced to V_{SS})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 1)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	5.0	ΔV _{switch} ≤ 500 mV (5.), V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	—	800	—	250	1050	—	1200	Ω
		10		—	400	—	120	500	—	520	
		15		—	220	—	80	280	—	300	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (Figure 6)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	C _{I/O}	—		—	—	—	0.47	—	—	—	pF

- Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
- For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14066B

ELECTRICAL CHARACTERISTICS (6.) ($C_L = 50$ pF, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Times Input to Output ($R_L = 10$ k Ω) $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 15.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 6.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 4.0 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	20 10 7.0	40 20 15	ns
Control to Output ($R_L = 1$ k Ω) (Figure 2) Output "1" to High Impedance	t_{PHZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
Output "0" to High Impedance	t_{PLZ}	5.0 10 15	— — —	40 35 30	80 70 60	ns
High Impedance to Output "1"	t_{PZH}	5.0 10 15	— — —	60 20 15	120 40 30	ns
High Impedance to Output "0"	t_{PZL}	5.0 10 15	— — —	60 20 15	120 40 30	ns
Second Harmonic Distortion ($V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ k Ω , $f = 1.0$ kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) ($R_L = 1$ k Ω , 20 Log (V_{out}/V_{in}) = -3 dB, $C_L = 50$ pF, $V_{in} = 5$ V $_{p-p}$)	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) ($V_{in} = 5$ V $_{p-p}$, $R_L = 1$ k Ω , $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	-50	—	dB
Channel Separation (Figure 4) ($V_{in} = 5$ V $_{p-p}$, $R_L = 1$ k Ω , $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	-50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) ($R_1 = 1$ k Ω , $R_L = 10$ k Ω , Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV $_{p-p}$

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TEST CIRCUITS

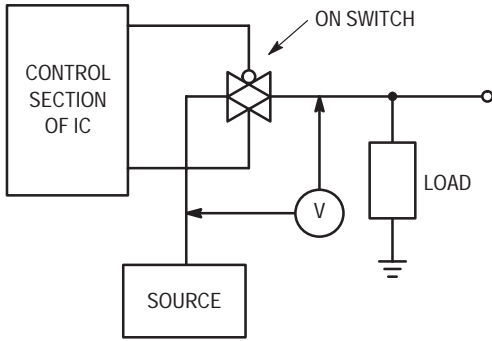


Figure 1. ΔV Across Switch

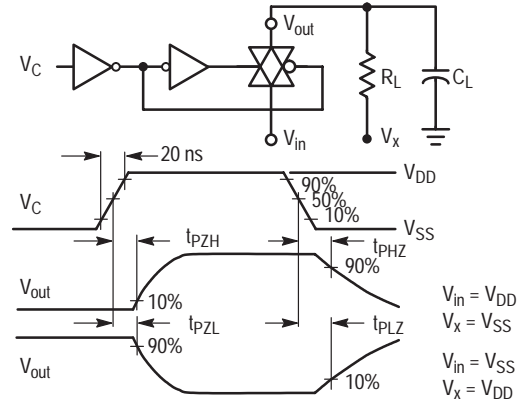


Figure 2. Turn-On Delay Time Test Circuit and Waveforms

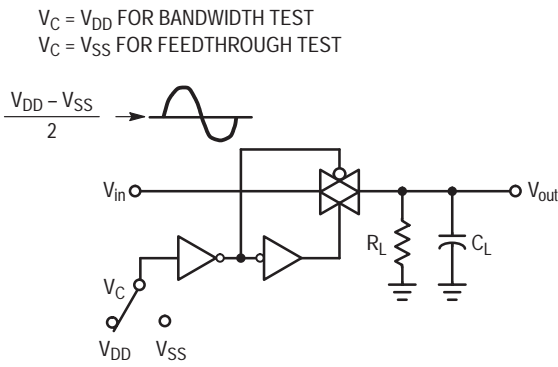


Figure 3. Bandwidth and Feedthrough Attenuation

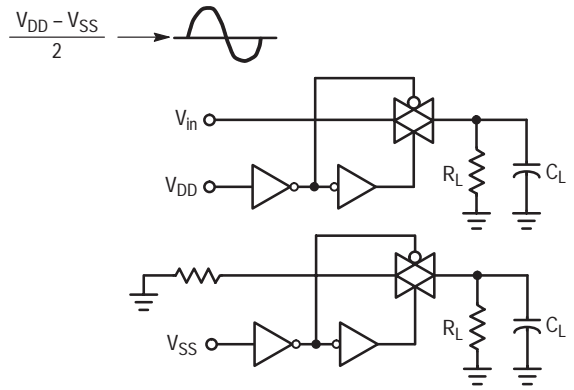


Figure 4. Channel Separation

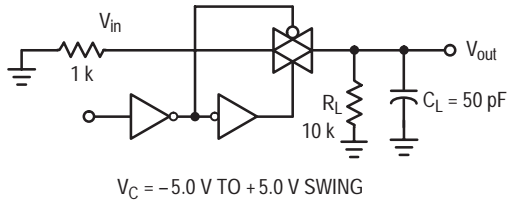


Figure 5. Crosstalk, Control to Output

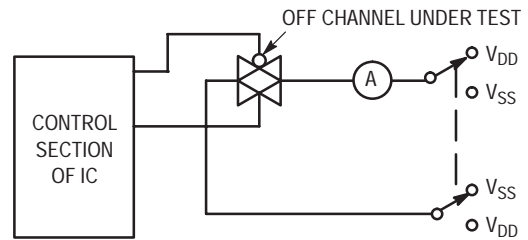


Figure 6. Off Channel Leakage

MC14066B

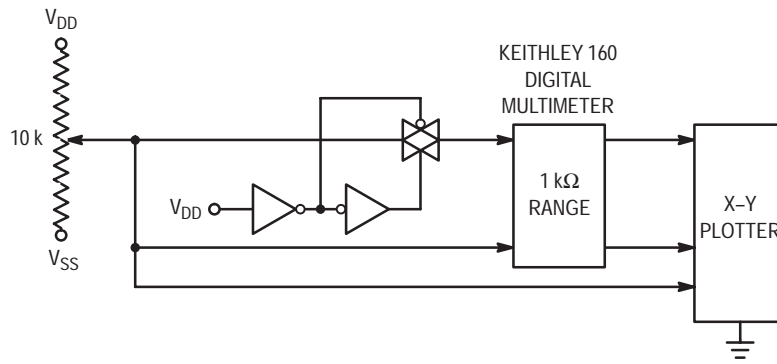


Figure 7. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

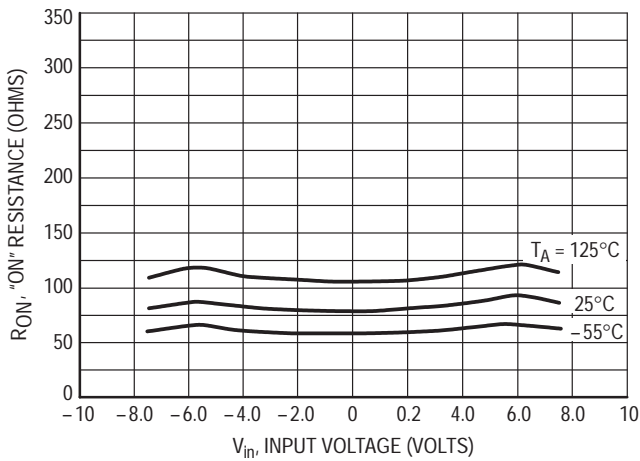


Figure 8. $V_{DD} = 7.5\text{ V}$, $V_{SS} = -7.5\text{ V}$

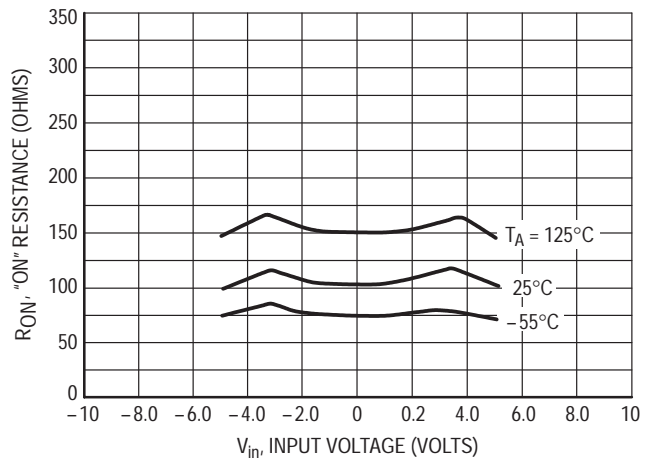


Figure 9. $V_{DD} = 5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$

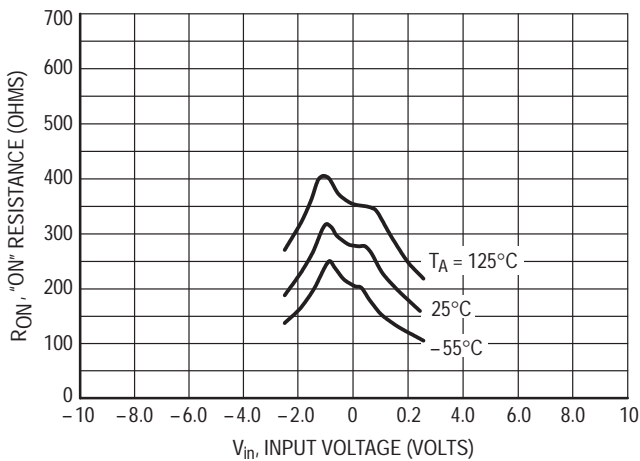


Figure 10. $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$

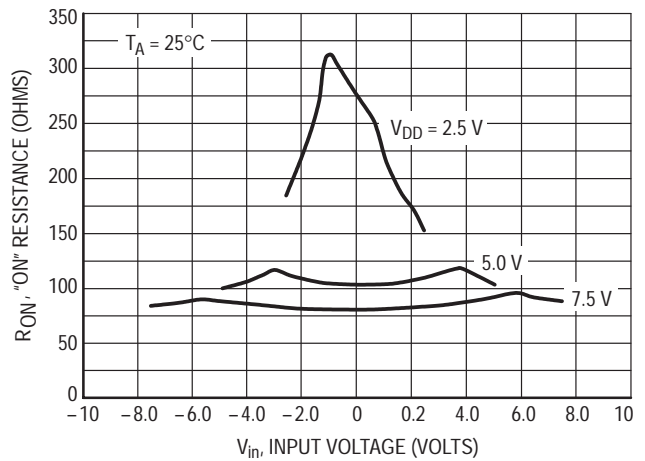


Figure 11. Comparison at 25°C , $V_{DD} = -V_{SS}$

MC14066B

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–5 volt digital control signal is used to directly control a 5 volt peak–to–peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS} . The V_{DD} voltage is the logic high voltage, the V_{SS} voltage is logic low. For the example, $V_{DD} = +5\text{ V} =$ logic high at the control inputs; $V_{SS} = \text{GND} = 0\text{ V} =$ logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS} . The analog voltage must not swing higher than V_{DD} or lower than V_{SS} .

The example shows a 5 volt peak–to–peak signal which allows no margin at either peak. If voltage transients above

V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS} .

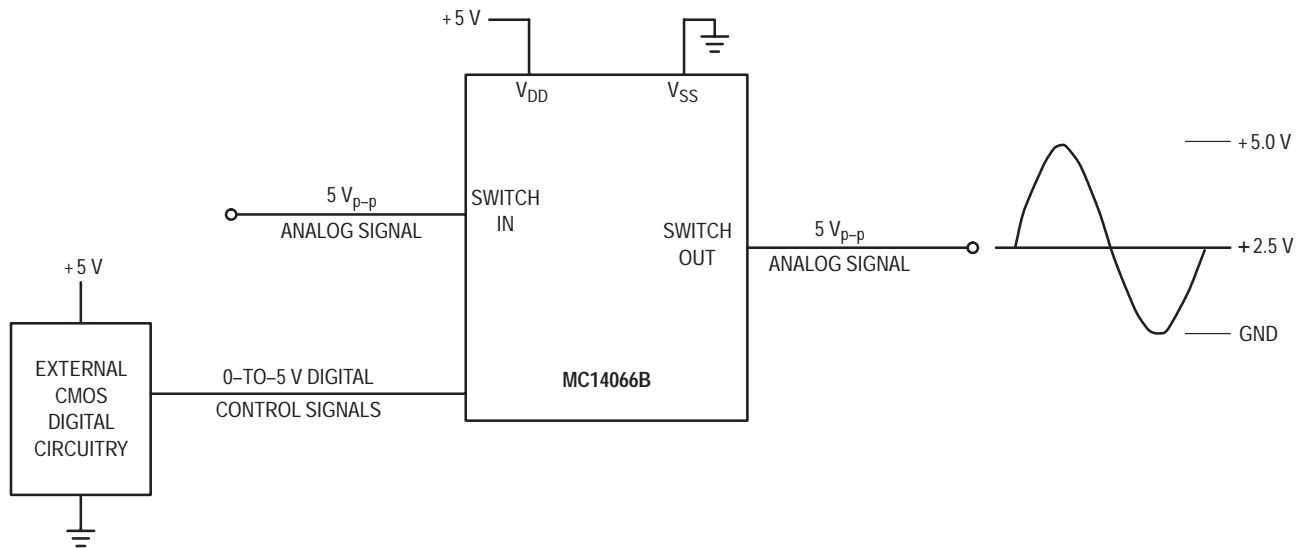


Figure A. Application Example

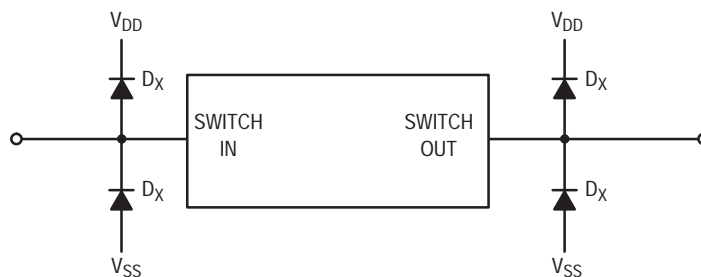
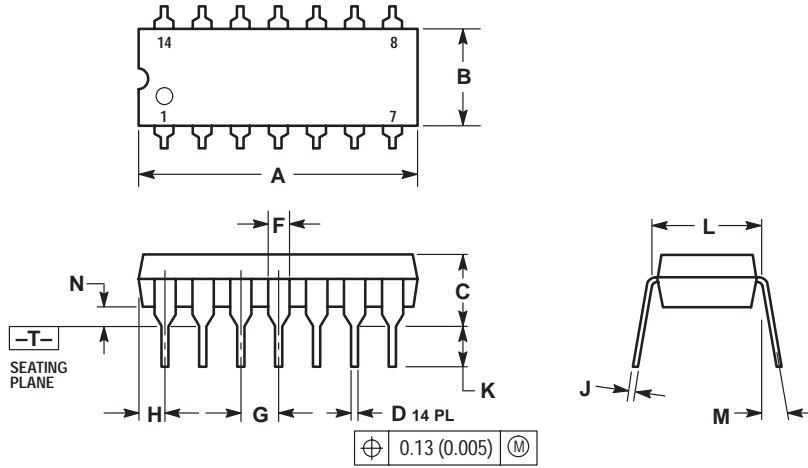


Figure B. External Germanium or Schottky Clipping Diodes

MC14066B

PACKAGE DIMENSIONS

P SUFFIX
PLASTIC DIP PACKAGE
CASE 646-06
ISSUE M



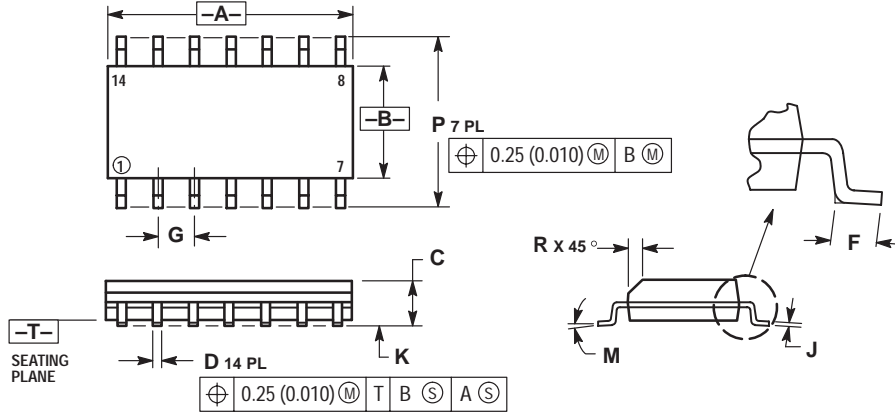
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

MC14066B

PACKAGE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



NOTES:

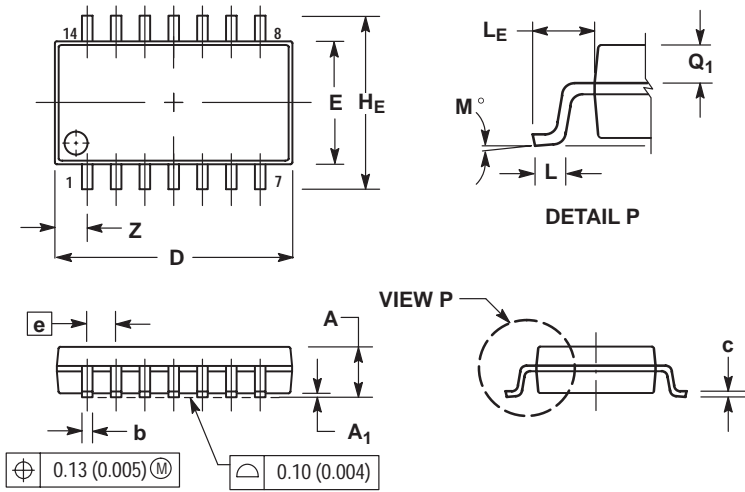
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC14066B

PACKAGE DIMENSIONS

F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 965-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _F	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	—	1.42	—	0.056

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